AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application.

COMPLETE LISTING OF CLAIMS:

Claims 1-19 : (Canceled)

Claim 20 : (Currently Amended) A switching network for switching frames of data, in defined time-slots, of a cross-connection request between a desired input and a desired output, comprising: an input stage having a plurality of switching matrices, an intermediate stage having a plurality of switching matrices, and an output stage having a plurality of switching matrices, each input stage switching matrix having a link to each intermediate stage switching matrix, and each intermediate stage switching matrix having a link to each output stage switching matrix, including ~~means~~ a controller for routing each time-slot of each frame independently through the switching matrices.

Claim 21 : (Currently Amended) The switching network as claimed in claim 20, in which the routing ~~means~~ controller is arranged to route each succeeding time-slot of the cross-connection request frame through the intermediate stage switching matrix having the link with the largest instantaneous number of free time-slots.

Claim 22 : (Previously Presented) The switching network as claimed in claim 21, in which the links are between the intermediate stage switching matrix and the output stage switching matrix of the requested output.

Claim 23 : (Currently Amended) The switching network as claimed in claim 22, in which the routing ~~means~~ controller is arranged to route each succeeding time-

slot through the intermediate stage switching matrix having the link from the input stage switching matrix at which the request was received with the largest instantaneous number of free time-slots, in the event that a plurality of intermediate stage switching matrices have equal instantaneous numbers of free time-slots in the links to the output stage switching matrices.

Claim 24 : (Currently Amended) The switching network as claimed in claim 20, in which the routing ~~means~~ controller is arranged to create a list of free time-slots in the links between the intermediate stage switching matrices and the input and output stage switching matrices of the request when the cross-connection request is received.

Claim 25 : (Currently Amended) The switching network as claimed in claim 20, in which the ~~inks~~ links are time division multiplex links.

Claim 26 : (Previously Presented) The switching network as claimed in claim 20, in which the number of intermediate stage switching matrices is at least two less than the sum of the number of inputs of each input stage switching matrix and outputs of each output stage switching matrix.

Claim 27 : (Previously Presented) The switching network as claimed in claim 20, in which the number of intermediate stage switching matrices is less than twice the number of inputs of each input stage switching matrix.

Claim 28 : (Previously Presented) The switching network as claimed in claim 27, in which the number of intermediate stage switching matrices is less than one and one half times the number of inputs of each input stage switching matrix.

Claim 29 : (Currently Amended) The switching network as claimed in claim 20, in which the routing ~~means~~ controller is arranged to reassemble the individually-routed time-slots into frames at the output of the output stage switching matrices.

Claim 30 : (Currently Amended) The switching network as claimed in claim 20, in which the switching matrices are ~~adapted~~ arranged to receive standard data traffic from which internally-generated frames replacing at least some overhead have been created.

Claim 31 : (Previously Presented) The switching network as claimed in claim 20, in which each time-slot of the links corresponds to a frame having a data rate at least one sixteenth of that of the links.

Claim 32 : (Previously Presented) The switching network as claimed in claim 31, in which the time-slots can each accommodate an AU-3 frame of the synchronous digital hierarchy standard.

Claim 33 : (Currently Amended) A digital cross-connect, comprising: a switching network for switching frames of data, in defined time-slots, of a cross-connection request between a desired input and a desired output, the switching network including an input stage having a plurality of switching matrices, an intermediate stage having a plurality of switching matrices, and an output stage having a plurality of switching matrices, each input stage switching matrix having a link to each intermediate stage switching matrix, and each intermediate stage switching matrix having a link to each output stage switching matrix, including ~~means~~ a controller for routing each time-slot of each frame independently through the switching matrices.

Claim 34 : (Previously Presented) A method of routing frames of data in defined time-slots through a switching network to fulfil a cross-connection request between

a desired input and a desired output, wherein the switching network comprises an input stage having a plurality of switching matrices, an intermediate stage having a plurality of switching matrices, and an output stage having a plurality of switching matrices, each input stage switching matrix having a link to each intermediate stage switching matrix, and each intermediate stage switching matrix having a link to each output stage switching matrix, the method comprising the step of: routing each time-slot of each frame independently through the switching matrices.

Claim 35 : (Previously Presented) The method as claimed in claim 34, in which the routing step is performed by routing each succeeding time-slot of the cross-connection request frame through the intermediate stage switching matrix having the link with the largest instantaneous number of free time-slots.

Claim 36 : (Previously Presented) The method as claimed in claim 35, in which the links are between the intermediate stage switching matrix and the output stage switching matrix of the requested output.

Claim 37 : (Previously Presented) The method as claimed in claim 36, in which the routing step is performed by routing each succeeding time-slot through the intermediate stage switching matrix having the link from the input stage switching matrix at which the request was received with the largest instantaneous number of free time-slots, in the event that a plurality of intermediate stage switching matrices have equal instantaneous numbers of free time-slots in the links to the output stage switching matrices.

Claim 38 : (Previously Presented) The method as claimed in claim 34, and the step of creating a list of free time-slots in the links between the intermediate stage switching matrices and the input and output stage switching matrices of the request when the cross-connection request is received.